Claims

1. A method to order memory operations in a system, the method comprising:

using at least one signal to indicate that a particular kind of memory operation is not globally observable but is observable by at least one processor of the system.

2. The method of claim 1, wherein using includes using at least two signals, wherein a first signal of the at least two signals indicates that a load operation issued by the at least one processor is not globally observable by all processors of the system but is observable by the at least one processor and wherein a second signal of the at least two signals indicates that a store operation issued by the at least one processor is not globally observable by all processors of the system but is observable by the at least one processor.

3. The method of claim 1, wherein using includes using at least three signals, wherein a first signal of the at least three signals indicates that a load operation issued by the at least one processor is not globally observable by all processors of the system but is observable by the at least one processor, wherein a second signal of the at least three signals indicates that a store operation issued by the at least one processor is not globally observable by all processors of the system but is observable by the at least one processor, wherein a third signal of the at least three signals indicates that a swap operation issued by the at least one processor is not globally observable by all processors of the system but is observable by the at least one processor.

4. The method of claim 1, further comprising dividing a memory space of the system into at least two regions and using at least two signals for each region of the at least two regions, wherein each signal of the at least two signals is associated with a particular kind of memory operation to one region of the at least two regions and indicates that the particular kind of memory operation is not globally observable in the system but is observable by at least one processor of the system.

5. The method of claim 1, wherein using includes using a first signal to indicate that a store operation issued by the at least one processor is not globally observable by all processors of the system.

6. The method of claim 5, further comprising asserting the first signal to indicate that the store operation is not globally observable by all processors of the system but is observable by the at least one processor.

7. The method of claim 6, further comprising allowing other store operations to be issued by any of the processors of the system if the first signal is asserted.

8. The method of claim 6, further comprising preventing any processor of the system to issue a memory operation other than a store operation if the first signal is asserted.

9. The method of claim 6, further comprising preventing any processor of the system to issue a load operation or swap operation if the first signal is asserted.

10. The method of claim 6, further comprising deasserting the first signal after the store operation is globally observable by all processors of the system.

11. The method of claim 1, wherein using includes using a first signal to indicate that a load operation issued by the at least one processor is not globally observable by all processors of the system.

12. The method of claim 11, further comprising asserting the first signal to indicate that the load operation is not globally observable by all processors of the system but is observable by the at least one processor.

13. The method of claim 11, further comprising allowing other load operations to be issued by any of the processors of the system if the first signal is asserted.

14. The method of claim 11, further comprising preventing any processor of the system to issue a memory operation other than a load operation if the first signal is asserted.

15. The method of claim 11, further comprising preventing any processor of the system to issue a store operation or swap operation if the first signal is asserted.

16. The method of claim 11, further comprising deasserting the first signal after the load operation is globally observable by all processors of the system.

17. The method of claim 1, wherein using includes using a first signal to indicate that a swap operation issued by the at least one processor is not globally observable by all processors of the system.

18. The method of claim 17, further comprising asserting the first signal to indicate that the swap operation is not globally observable by all processors of the system but is observable by the at least one processor.

19. The method of claim 17, further comprising preventing any processor of the system to issue any memory operation if the first signal is asserted.

20. The method of claim 17, further comprising preventing any processor of the system to issue a load operation, a store operation, or a swap operation if the first signal is asserted.

21. The method of claim 17, further comprising deasserting the first signal after the swap operation is globally observable by all processors of the system.

22. A system, comprising:

a first processor to use at least one signal for memory consistency, wherein the at least one signal indicates that a particular kind of memory operation is not globally observable in the system but is observable by at least one processor of the system.

23. The system of claim 22, further comprising:

a second processor coupled to the first processor;

a first signal line coupled to the first processor and the second processor;

a second signal line coupled to the first processor and the second processor; and

a third signal line coupled to the first processor and the second processor.

24. The system of claim 23, wherein the first processor has logic to assert the first signal line after the first processor issues a load operation to indicate that the load operation is not globally observable in the system but is observable by at least one processor of the system.

25. The system of claim 24, wherein the second processor has logic to prevent the second processor from issuing a memory operation other than a load operation while the first signal line is asserted.

26. The system of claim 24, wherein the second processor has logic to prevent the second processor from issuing a store operation or a swap operation while the first signal line is asserted.

27. The system of claim 23, wherein the first processor has logic to assert the second signal line after the first processor issues a store operation to indicate that the store operation is not globally observable in the system but is observable by at least one processor of the system.

28. The system of claim 27, wherein the second processor has logic to prevent the second processor from issuing a memory operation other than a store operation while the second signal line is asserted.

29. The system of claim 27, wherein the second processor has logic to prevent the second processor from issuing a load operation or a swap operation while the second signal line is asserted.

30. The system of claim 24, wherein the first processor has logic to assert the third signal line after the first processor issues a swap operation to indicate that the swap operation is not globally observable in the system but is observable by at least one processor of the system.

31. The system of claim 30, wherein the second processor has logic to prevent the second processor from issuing any memory operation while the third signal line is asserted.

32. The system of claim 30, wherein the second processor has logic to prevent the second processor from issuing a store operation, a load operation, or a swap operation while the third signal line is asserted.

33. The system of claim 23, further comprising:

a fourth signal line coupled to the first processor and the second processor;

a fifth signal line coupled to the first processor and the second processor; and

a sixth signal line coupled to the first processor and the second processor.

34. The system of claim 33, wherein the first processor has logic to assert the first signal line after the first processor issues a load operation to a first region of a memory of the system, wherein asserting the first signal line indicates that the load operation is not globally observable but is observable by the at least one processor.

35. The system of claim 34, wherein the first processor has logic to assert the second signal line after the first processor issues a load operation to a second region of the memory of the system, wherein asserting the second signal line indicates that the load operation is not globally observable but is observable by the at least one processor.

36. The system of claim 33, wherein the first processor has logic to assert the third signal line after the first processor issues a store operation to a first region of a memory of the system, wherein asserting the third signal line indicates that the store operation is not globally observable but is observable by the at least one processor.

37. The system of claim 36, wherein the first processor has logic to assert the fourth signal line after the first processor issues a store operation to a second region of the memory of the system, wherein asserting the fourth signal line indicates that the store operation is not globally observable but is observable by the at least one processor.

38. The system of claim 33, wherein the first processor has logic to assert the fifth signal line after the first processor issues a swap operation to a first region of a memory of the system, wherein asserting the fifth signal line indicates that the swap operation is not globally observable but is observable by the at least one processor.

39. The system of claim 38, wherein the first processor has logic to assert the sixth signal line after the first processor issues a swap operation to a second region of the memory of the system, wherein asserting the sixth signal line indicates that the swap operation is not globally observable but is observable by the at least one processor.

40. The system of claim 22, wherein the first processor and second processor are integrated together on a single silicon die.

41. The system of claim 22, further comprising:

a first local cache memory coupled to the first processor;

a second local cache memory coupled to the second processor; and

a shared cache memory, wherein the shared cache memory is coupled to the first processor via the first local cache and the shared cache is coupled to the second processor via the second local cache.

42. A system, comprising:

a first processor to use at least one signal for memory consistency, wherein the at least one signal indicates that a particular kind of memory operation is not globally observable in the system but is observable by at least one processor of the system; and

an antenna coupled to the first processor.

43. The system of claim 42, further comprising:

a second processor coupled to the first processor;

a first signal line coupled to the first processor and the second processor;

a second signal line coupled to the first processor and the second processor; and

a third signal line coupled to the first processor and the second processor.

44. The system of claim 43, wherein the first processor has logic to assert the first signal line after the first processor issues a load operation to indicate that the load operation is not globally observable in the system but is observable by at least one processor of the system.

45. The system of claim 42, wherein the system is a wireless phone.